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10/002,869	12/05/2001	B. Arlen Young	ADPT1049	4797

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EXAMINER	
PATEL, NIMESH G	

ART UNIT	PAPER NUMBER
2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/002,869	Applicant(s) YOUNG, B. ARLEN	
	Examiner Nimesh G Patel	Art Unit 2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-15 and 17-20* is/are rejected.

7)☒ Claim(s) *2 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 6-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art, in view of Gates et al.('482), hereinafter referred to as Gates.

3. Regarding claim 1, the admitted prior art discloses a method for using a hardware I/O control block array by a parallel SCSI host adapter(Page 1, Lines 18-25).

The admitted prior art does not disclose a method comprising: partitioning said hardware I/O control block array for said parallel SCSI host adapter into first and second pages; using only said first page for non-Packetized SCSI Protocol hardware I/O control block storage; and using said first and second pages for Packetized SCSI Protocol hardware I/O control block storage. However, Gates discloses a method for partitioning memory into sections depending on the type of information(Column 4, Lines 1-6; One section, i.e. a page since only one page can exist in a section, could be used for non-Packetized SCSI Protocol hardware I/O control block storage and another section could be used for Packetized SCSI Protocol hardware I/O control block storage). Therefore it would have been obvious to use the teachings of Gates in the system of the admitted prior art to partition said hardware I/O control block array for said parallel SCSI host adapter into first and second pages; using only said first page for non-Packetized SCSI Protocol hardware I/O control block storage; and using said first and second pages for Packetized SCSI Protocol hardware I/O control block storage to minimize the number

of address bits required for an internal address space of a circuit and does not require frequent page changes to locate required information(Column 3, Lines 59-63).

4. Regarding claim 6, Gates discloses a method further comprising: using a hardware I/O control block array pointer having a low byte and a high byte to address a storage site in said hardware I/O control block array(Column 3, Lines 52-53; Column 10, Lines 1-20; Column 11, Lines 63-65).

5. Regarding claim 7, the admitted prior art discloses a method further comprising: loading a tag from a reconnecting target into said low byte only(Page 2, Line 23 – Page 3, Line 4).

6. Regarding claim 8, Gates discloses a method further comprising: loading said high byte with a zero value(Column 10, Lines 53-54).

7. Regarding claim 9, the admitted prior art does not disclose a method further comprising: loading a tag from a reconnecting target into said low byte and said high byte. However it would be inherent to load a high byte and a low byte of tag that is two bytes into a two-byte pointer.

8. Regarding claim 10, the admitted prior art discloses a system comprising: a parallel SCSI host adapter comprising; a sequencer; and a hardware I/O control block array pointer, coupled to said sequencer; and a memory, coupled to said hardware I/O control block array pointer(Page 1, Lines 18-31) and a plurality of hardware I/O control block storage sites equal to a number of unique tag values that can be returned by a non-Packetized SCSI Protocol tagged queue target reconnecting to said parallel SCSI host adapter(Page 2, Line 23 – Page 3, Line 4).

The admitted prior art does not disclose said pointer having a low byte and a high byte; and a hardware I/O control block array comprising: a plurality of pages including a first page and a second page, wherein; and said second page includes another plurality of hardware I/O control block storage sites. However, Gates discloses a method for partitioning memory into sections depending on the type of information(Column 4, Lines 1-6; One section, i.e. a page

since only one page can exist in a section, could be used for non-Packetized SCSI Protocol hardware I/O control block storage and another section could be used for Packetized SCSI Protocol hardware I/O control block storage). Therefore it would have been obvious to use the teachings of Gates in the system of the admitted prior art to partition said hardware I/O control block array for said parallel SCSI host adapter into first and second pages to minimize the number of address bits required for an internal address space of a circuit and does not require frequent page changes to locate required information(Column 3, Lines 59-63).

9. Regarding claim 11, Gates disclose a system, wherein said memory is external to said parallel SCSI host adapter(Figure 1).

10. Regarding claim 12, the admitted prior art and Gates do not disclose a system, wherein said memory is internal to said parallel SCSI host adapter. However, it is well known in the art to have memory internal in a host adapter and the system of the admitted prior art and Gates could function the same if the memory was internal.

11. Regarding claim 13, the admitted prior art disclose a system 10 further comprising: a driver coupled to said parallel SCSI host adapter, wherein said driver allocates and de-allocates storage sites in said hardware I/O control block array(Page 1, Lines 21-26).

12. Regarding claim 14, Gates disclose a system, wherein said driver allocates sites for non-Packetized SCSI hardware I/O control blocks only in said first page(Column 4, Lines 1-3; Memory is divided into sections dedicated for different types of information, i.e. non-Packetized SCSI hardware I/O control blocks only in a first section, i.e. first page since only one page can exist in a section).

13. Regarding claim 15, Gates discloses a system wherein said driver allocates sites for Packetized SCSI hardware I/O control blocks in said first page and in said second page(Column 4, Lines 1-3; memory sections are divided into pages. I.e. first page and second page).

14. Claims 3-5, 17-19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art, in view of Gates et al.('482), and in further view of Percival('136).

15. Regarding claim 3, the admitted prior art and Gates do not disclose a method further comprising: maintaining a first page free site queue for said first page by a driver for said parallel SCSI host adapter. However, Percival discloses using a free queue to allocate memory for a control block(Column 4, Lines 30-33). Therefore it would have been obvious to use the teachings of Percival in the system of the admitted prior art and Gates, to maintain a first page free site queue for said first page by a driver since this would inform the system what memory locations are free to use in the first page.

16. Regarding claim 4, Pecival disclose maintaining a second page free site queue for said second page by said driver for said parallel SCSI host adapter(Column 4, Lines 30-33).

17. Regarding claim 5, Pecival discloses a method further comprising: maintaining a second page free site queue for said second page by a driver for said parallel SCSI host adapter(Column 4, Lines 30-33).

18. Regarding claim 17, the admitted prior art and Gates do not disclose a system further comprising: a first page free site queue coupled to said driver. However, Percival discloses using a free queue to allocate memory for a control block(Column 4, Lines 30-33). Therefore it would have been obvious to use the teachings of Percival in the system of the admitted prior art and Gates, to maintain a first page free site queue for said first page by a driver since this would inform the system what memory locations are free to use in the first page.

19. Regarding claim 18, Percival discloses a system further comprising: a second page free site queue coupled to said driver(Column 4, Lines 30-33).

20. Regarding claim 19, Percival disclose a system further comprising: a second page free site queue coupled to said driver(Column 4, Lines 30-33).

21. Regarding claim 20, the admitted prior art discloses a method for using a hardware I/O control block array by a parallel SCSI host adapter, said method comprising: loading a tag from a reconnecting target into said hardware I/O control block array pointer(Page 1, Lines 18-21; Page 2, Line 23 – Page 3, Line 4).

The admitted prior art does not disclose partitioning said hardware I/O control block array for said parallel SCSI host adapter into first and second pages; and using only said first page for non-Packetized SCSI protocol hardware I/O control block storage; using said first and second pages for Packetized SCSI Protocol hardware I/O control block storage. However, Gates discloses a method for partitioning memory into sections depending on the type of information(Column 4, Lines 1-6; One section, i.e. a page since only one page can exist in a section, could be used for non-Packetized SCSI Protocol hardware I/O control block storage and another section could be used for Packetized SCSI Protocol hardware I/O control block storage). Therefore it would have been obvious to use the teachings of Gates in the system of the admitted prior art to partition said hardware I/O control block array for said parallel SCSI host adapter into first and second pages to minimize the number of address bits required for an internal address space of a circuit and does not require frequent page changes to locate required information(Column 3, Lines 59-63). Gates further discloses using a hardware I/O control block array pointer having a low byte and a high byte to address a storage site in said hardware I/O control block array(Column 3, Lines 52-53; Column 10, Lines 1-20; Column 11, Lines 63-65)

The admitted prior art and Gates do not disclose maintaining a first page free site queue for said first page by a driver for said parallel SCSI host adapter; maintaining a second page free site queue for said second page by said driver for said parallel SCSI host adapter. However, Percival discloses using a free queue to allocate memory for a control block(Column

4, Lines 30-33). Therefore it would have been obvious to use the teachings of Percival in the system of the admitted prior art and Gates, to maintain a first page free site queue for said first page by a driver since this would inform the system what memory locations are free to use in the first page.

Allowable Subject Matter

22. Claims 2 and 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The references cited further disclose art related to host adaptors using hardware control blocks and art related to partitioning memory.

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nimesh G Patel whose telephone number is 703-305-7583. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nimesh G Patel
Examiner
Art Unit 2112

NP NP
May 3, 2004

Glenn A. Auve
Primary Patent Examiner
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